

REMARKS

The Office Action mailed April 22, 2002 requires a restriction to one of the following groups of claims:

I. Claims 1-55;

II. Claim 56.

Applicants elect Claims 1-55.

The specification is amended to improve grammar.

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Michael Shenker 5-21-02
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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Version with Markings to Show Changes Made

IN THE SPECIFICATION

Please amend the paragraph on page 1, line 25, through page 2, line 4, to read as follows:

The input and output registers however, cause two clock cycles of latency in the relation between the read address and read data, and no latency between the write address and write data (i.e., the address is clocked in and the data is clocked out in two consecutive clock cycles for a read, and the address and data are clocked in in the same clock cycle for a write). This latency difference between read and write operations causes the address bus to remain idle for two clock cycles when a read cycle is followed by a write cycle, and causes the data bus to remain idle for two clock cycles when a write cycle is followed by a read cycle (i.e., bus turnaround). The idle cycles reduce the system data bandwidth.